

Notice of Allowability

Application No.

10/025,870

Examiner

Chat C. Do

Applicant(s)

JIN ET AL.

Art Unit

2193

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 02/17/2005.
2. ☒ The allowed claim(s) is/are 10-14,27,30-36 and 41.
3. ☒ The drawings filed on 26 December 2001 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date attached.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Victoria Donnelly on 05/16/2005.

The application has been amended as follows in order to overcome the cited prior art as discussed with the examiner in the telephone interview dated above:

Claim 9. (canceled)

Claim 10. (~~Original~~ Currently Amended) A method of performing a k-stage FFT computation of N data points wherein k and N are integers, the method comprising: for each one of a plurality of stage groupings of at least one stage of k stages of the k-stage FFT computation wherein the plurality of stage groupings of at least one stage collectively comprise the k stages, performing a respective plurality of operations on the N data points, each one of the respective plurality of operations comprising: performing an import of a respective plurality of sets of data points of the N data points from an external memory into an internal memory; performing a FFT computation upon each one of the respective plurality of sets of data points of the N data points in the internal memory; and performing an export of the respective plurality of sets of data points of the

N data points from the internal memory into the external memory to update the respective plurality of sets of data points of the N data points in the external memory; wherein the stage groupings of at least one stage comprise Q stage groupings each comprising S stages, said Q and said S being integers with $Q \geq 1$, $S \geq 1$ and $k \geq QS$; and wherein N substantially satisfies $N = 2^k$, comprising:

grouping, within a stage grouping, I, of the Q stage groupings wherein I is an integer satisfying $0 \leq I \leq Q-1$, the N data points into 2^{IS} blocks of data of $N/2^{IS}$ respective data points;

grouping, within each one of the 2^{IS} blocks of data, the $N/2^{IS}$ respective data points into 2^S sub-blocks of data of $N/2^{IS+S}$ respective data points;

grouping, within each one of the 2^S sub-blocks of data, the $N/2^{IS+S}$ respective data points into M_1 sub-sub-blocks of data of $N/(2^{IS+S} M_1)$ respective data points wherein M_1 is an integer;

taking, within each one of the 2^{IS} blocks of data, a respective sub-sub-block of data of the M_1 sub-sub-blocks of data from each one of the 2^S sub-blocks of data to form a set of 2^S sub-sub-blocks of data of $N/(2^{IS} M_1)$ data points a total of M_1 times to produce M_1 sets of 2^S sub-sub-blocks of data of $N/(2^{IS} M_1)$ data points;

taking, within each one of the M_1 sets of 2^S sub-sub-blocks of data, a respective data point from each one of the 2^S sub-blocks of data to form a set of 2^S data points a total of $N/(2^{IS+S} M_1)$ times to produce $N/(2^{IS+S} M_1)$ sets of 2^S data points;

wherein, for the stage grouping, I, of the of the Q stage groupings of the plurality of stage groupings, the performing a respective plurality of operations on the N data

points comprises performing M_1 of the plurality of operations for each one of the 2^{1S} blocks of data within the stage grouping, I, each one of the M_1 of the plurality operations comprising:

performing an import of respective $N/(2^{1S+S}M_1)$ sets of 2^S data points from the external memory into the internal memory;

performing an S-stage FFT computation of the k-stage FFT computation upon each set of 2^S data points of the respective $N/(2^{1S+S}M_1)$ sets of 2^S data points in the internal memory;

performing an export of the respective $N/(2^{1S+S}M_1)$ sets of 2^S data points from the internal memory into the external memory to update the respective $N/(2^{1S+S}M_1)$ sets of 2^S data points in the external memory;

wherein the internal memory comprises a double buffer adapted to store the plurality of sets of data points, wherein the double buffer comprises two buffers each capable of storing $M_1/2$ data points and wherein said M_1 substantially satisfies $M_1 = N/(2^{1S-1}M_1)$, M_1 being an integer.

Claim 11. (~~Original~~ Currently Amended) A method of performing a k-stage FFT computation according to claim 10 wherein M_1 substantially satisfies $M_1 = N/(2^{1S}M_1)$ wherein M_1 corresponds to the number of data points the internal memory ~~can hold~~ is capable of holding.

Claim 12. (~~Original~~ Currently Amended) A method of performing a k-stage FFT computation according to claim 10 wherein M_1 substantially satisfies $M_1 = N/(2^{1S-1}M_1)$ wherein M_1 corresponds to the number of data points a buffer in the internal memory ~~can~~ hold is capable of holding.

Claim 26. (canceled)

27. (~~Original~~ Currently Amended) A processor comprising an internal memory adapted to store data; a DMA (direct memory access) unit adapted to import data into the internal memory and to export data from the internal memory; and a central processor unit (CPU) adapted to perform, for each one of a plurality of stage groupings of at least one stage of k stages of the k-stage FFT computation wherein the plurality of stage groupings of at least one stage collectively comprise the k stages, a respective plurality of operations on the N data points, for each one of the respective plurality of operations the CPU is adapted to: provide instructions to the DMA unit for performing an import of a respective plurality of sets of data points, of N data points, into the internal memory; perform a FFT computation upon each one of the respective plurality of sets of data points, of the N data points, in the internal memory; and provide instructions to the DMA unit for performing an export of the respective plurality of sets of data points, of the N data points, from the internal memory to update the respective plurality of sets of data points of the N data points, wherein the CPU is adapted to:

group, within a stage grouping, I, of the Q stage groupings wherein I is an integer satisfying $0 \leq I \leq Q-1$, the N data points into 2^{IS} blocks of data of $N/2^{IS}$ respective data points;

group, within each one of the 2^{IS} blocks of data, the $N/2^{IS}$ respective data points into 2^S sub-blocks of data of $N/2^{IS+S}$ respective data points;

group, within each one of the 2^S sub-blocks of data, the $N/2^{IS+S}$ respective data points into M_1 sub-sub-blocks of data of $N/(2^{IS+S} M_1)$ respective data points wherein M_1 is an integer;

take, within each one of the 2^{IS} blocks of data, a respective sub-sub-block of data of the M_1 sub-sub-blocks of data from each one of the 2^S sub-blocks of data to form a set of 2^S sub-sub-blocks of data of $N/(2^{IS} M_1)$ data points a total of M_1 times to produce M_1 sets of 2^S sub-sub-blocks of data of $N/(2^{IS} M_1)$ data points; and

take, within each one of the M_1 sets of 2^S sub-sub-blocks of data, a respective data point from each one of the 2^S sub-blocks of data to form a set of 2^S data points a total of $N/(2^{IS+S} M_1)$ times to produce $N/(2^{IS+S} M_1)$ sets of 2^S data points;

wherein, for the stage grouping, I, of the of the Q stage groupings of the plurality of stage groupings, the CPU is adapted to perform M_1 of the plurality operations for each one of the 2^{IS} blocks of data within the stage grouping, I, and for each one of the M_1 of the plurality operations the CPU is adapted to: provide instructions to the DMA unit for performing an import of respective $N/(2^{IS+S} M_1)$ sets of 2^S data points into the internal memory;

performing an S-stage FFT computation of the k-stage FFT computation upon each set of 2^S data points of the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points in the internal memory; and

provide instructions to the DMA unit for performing an export of the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points from the internal memory to update the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points;

wherein the internal memory comprises a buffer adapted to store the plurality of sets of data points, wherein the buffer has a capacity to hold M_1 data points and M_1 substantially satisfies $M_1 = N/(2^{IS}M_1)$ wherein M_1 is an integer; and

wherein the internal memory comprises a double buffer adapted to store the plurality of sets of data points, wherein the double buffer comprises two buffers each capable of storing $M_1/2$ data points and wherein said M_1 substantially satisfies $M_1 = N/(2^{IS-1}M_1)$, M_1 being an integer.

Claim 28. (canceled)

Claim 29. (canceled)

Claim 30. (~~Original~~ Currently Amended) A processor according to claim 29 ~~27~~ wherein while the CPU performs the S-stage FFT computation of the k-stage FFT computation upon each set of 2^S data points of the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points, the respective $N/(2^{IS+S}M_1)$ sets of 2^S data points being stored in one of the two buffers, the

CPU is adapted to provide instructions to the DMA unit to import, into another one of the two buffers, respective $N/(2^{1S+S}M_1)$ sets of 2^S data points of a next one of the each one of the M_1 of the plurality operations.

Claim 31. (~~Original~~ Currently Amended) A processor according to claim ~~29~~ 27 wherein while the CPU performs the S-stage FFT computation of the k-stage FFT computation upon each set of 2^S data points of the respective $N/(2^{1S+S}M_1)$ sets of 2^S data points, the respective $N/(2^{1S+S}M_1)$ sets of 2^S data points being stored in one of the two buffers, the CPU is adapted to provide instructions to the DMA unit to export, from another one of the two buffers, respective $N/(2^{1S+S}M_1)$ sets of 2^S data points from previous one of the each one of the M_1 of the plurality operations.

Claim 35. (~~Original~~ Currently Amended) A processor according to claim ~~28~~ 27 wherein the stage groupings of at least one stage comprise a stage grouping of D stage wherein D is an integer, said k substantially satisfying $k=QS+D$ and said D substantially satisfying $D \leq \log_2(M_1)$.

Claim 36. (~~Original~~ Currently Amended) A processor according to claim ~~29~~ 27 wherein the stage groupings of at least one stage comprise a stage grouping of D stage wherein D is an integer, said k substantially satisfying $k=QS+D$ and said D substantially satisfying $D \leq \log_2(M_1/2)$.

Claim 41. (Currently amended) An article of manufacture ~~according to claim 40~~
comprising a computer readable medium storing computer readable program code means
embodied therein for performing a k-stage FFT computation of N data points wherein k
and N are integers, the computer readable code means in said article of manufacture
comprising computer readable code FFT means for performing, for each one of a
plurality of stage groupings of at least one stage of k stages of the k-stage FFT
computation wherein the plurality of stage groupings of at least one stage collectively
comprise the k stages, a respective plurality of operations on the N data points, for each
one of the respective plurality of operations the computer readable code FFT means
comprising computer readable code means for providing instructions for performing an
import of a respective plurality of sets of data points of the N data points from an external
memory into an internal memory; computer readable code means for performing a FFT
computation upon each one of the respective plurality of sets of data points of the N data
points in the internal memory; and computer readable code means for providing
instructions for performing an export of the respective plurality of sets of data points of
the N data points from the internal memory into the external memory to update the
respective plurality of sets of data points of the N data points in the external memory,
wherein the stage groupings of at least one stage comprise a stage grouping of D stage
and Q stage groupings of S stages wherein D, Q and S are integers and wherein said k
substantially satisfies $k=QS+D$ and $k = \log_2(N)$, comprising further computer readable
code means for:

grouping, within a stage grouping, I , of the Q stage groupings wherein I is an integer satisfying $0 \leq I \leq Q-1$, the N data points into 2^{IS} blocks of data of $N/2^{IS}$ respective data points;

grouping, within each one of the 2^{IS} blocks of data, the $N/2^{IS}$ respective data points into 2^S sub-blocks of data of $N/2^{IS+S}$ respective data points;

grouping, within each one of the 2^S sub-blocks of data, the $N/2^{IS+S}$ respective data points into M_1 sub-sub-blocks of data of $N/(2^{IS+S} M_1)$ respective data points wherein M_1 is an integer;

taking, within each one of the 2^{IS} blocks of data, a respective sub-sub-block of data of the M_1 sub-sub-blocks of data from each one of the 2^S sub-blocks of data to form a set of 2^S sub-sub-blocks of data of $N/(2^{IS} M_1)$ data points a total of M_1 times to produce M_1 sets of 2^S sub-sub-blocks of data of $N/(2^{IS} M_1)$ data points; and

taking, within each one of the M_1 sets of 2^S sub-sub-blocks of data, a respective data point from each one of the 2^S sub-blocks of data to form a set of 2^S data points a total of $N/(2^{IS+S} M_1)$ times to produce $N/(2^{IS+S} M_1)$ sets of 2^S data points;

wherein, for the stage grouping, I , of the of the Q stage groupings of the plurality of stage groupings, the computer readable code FFT means is further adapted to perform M_1 of the plurality operations for each one of the 2^{IS} blocks of data within the stage grouping, I , and for each one of the M_1 of the plurality operations the computer readable code FFT means further comprising:

computer readable code means for providing instructions for performing an import of respective $N/(2^{1S+S}M_1)$ sets of 2^S data points from the external memory into the internal memory;

computer readable code means for performing an S-stage FFT computation of the k-stage FFT computation upon each set of 2^S data points of the respective $N/(2^{1S+S}M_1)$ sets of 2^S data points in the internal memory; and computer readable code means for providing instructions for performing an export of the respective $N/(2^{1S+S}M_1)$ sets of 2^S data points from the internal memory into the external memory to update the respective $N/(2^{1S+S}M_1)$ sets of 2^S data points in the external memory.

Claim 42. (canceled)

2. Claims 1-9, 15-26, 28-29, 37-40, and 42 are cancelled.
3. Claims 10-14, 27, 30-36, and 41 are allowed.

REASONS FOR ALLOWANCE

4. The following is an examiner's statement of reasons for allowance:

The prior art of records fails to disclose or render an obviousness of a method of performing a k-stage FFT computation of N data points wherein k and N are integers comprising: grouping stages wherein for each grouping stage, performing an import of respective of data from external memory into the internal memory; performing a FFT

computation in the internal memory, and performing an export of data points from the internal memory into the external memory to update the respective sets of data wherein the internal memory comprises a double buffer adapted to store the plurality of sets of data points, wherein the double buffer comprises two buffers each capable of storing $M_1/2$ data points and wherein M_1 substantially satisfies $M_1 = N/(2^{IS-1}M_1)$, M_1 being an integer as cited in independent claims 10, 27, and 41.

The closest found prior art is Nakai et al. (U.S. 6,115,728). Nakai et al. disclose a method of performing a k-stage FFT computation of N data points wherein k and N are integers comprising grouping stages wherein for each grouping stage, performing an import of respective of data from external memory into the internal memory; performing a FFT computation in the internal memory, and performing an export of data points from the internal memory into the external memory to update the respective sets of data.

Nakai et al. fail to disclose the internal memory comprises a double buffer adapted to store the plurality of sets of data points, wherein the double buffer comprises two buffers each capable of storing $M_1/2$ data points and wherein M_1 substantially satisfies $M_1 = N/(2^{IS-1}M_1)$, M_1 being an integer as cited above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

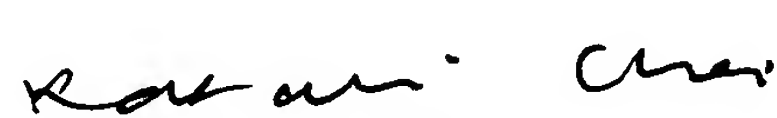
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on 7:00AM to 5:00PM M-Th.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C Do
Examiner
Art Unit 2193

May 23, 2005


KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100